



## **A 1.62GS/s Time-Interleaved SAR ADC with fully digital background mismatch calibration achieving interleaving spurs below 70dBFS**

Nicolas Le Dortz, J.-P. Blanc, Thierry Simon, Sarah Verhaeren, E. Rouat, Pascal Urard, S. Le Tual, D. Goguet, Caroline Lelandais-Perrault, Philippe Benabes

### **► To cite this version:**

Nicolas Le Dortz, J.-P. Blanc, Thierry Simon, Sarah Verhaeren, E. Rouat, et al.. A 1.62GS/s Time-Interleaved SAR ADC with fully digital background mismatch calibration achieving interleaving spurs below 70dBFS. ISSCC 2014, Feb 2014, San Francisco, United States. pp.386-388, 10.1109/ISSCC.2014.6757481 . hal-01075055

**HAL Id: hal-01075055**

**<https://hal-centralesupelec.archives-ouvertes.fr/hal-01075055>**

Submitted on 19 Jan 2015

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

## 22.5 A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs Below 70dBFS

Nicolas Le Dortz<sup>1,2</sup>, Jean-Pierre Blanc<sup>1</sup>, Thierry Simon<sup>1</sup>, Sarah Verhaeren<sup>1</sup>, Emmanuel Rouat<sup>1</sup>, Pascal Urard<sup>1</sup>, Stéphane Le Tual<sup>1</sup>, Dimitri Goguet<sup>1</sup>, Caroline Lelandais-Perrault<sup>2</sup>, Philippe Benabes<sup>2</sup>

<sup>1</sup>STMicroelectronics, Crolles, France, <sup>2</sup>Supélec, Gif-sur-Yvette, France

Today's applications such as broadband satellite receivers, cable TVs, and software-defined radios require highly efficient ADCs with high sampling rates and high resolutions. Time-interleaved ADC (TIADC) is a popular architecture used to achieve this goal. However, this structure suffers from mismatches between the sub-converters, which cause errors on the output signal and more significantly, decrease the SFDR. These mismatches can be a severe limitation in applications such as satellite reception where both narrowband and wideband signals are used. This paper introduces digital derivative-based estimation of timing mismatches. Gain, offset and skew mismatch calibrations are performed entirely in the digital domain through equalization.

Recently, multi-GS/s designs using mixed signal techniques to reduce the effects of mismatches have been published [1-3]. Mixed calibration techniques exhibit good performance but they require additional development time. This prototype, done in 40nm CMOS technology, implements a 1.62GS/s 12-channel 9-bit TIADC with embedded digital background mismatch calibration. It demonstrates the efficiency of a generalizable and scalable co-design methodology where the analog core is designed without special care for the mismatches. The mismatches are suppressed by a separately designed digital background mismatch calibration unit. Over the range 0-750MHz, the on-chip implementation of this architecture has interleaving spurs below 70 dBFS and a SNDR higher than 48dB for a power consumption of 93mW.

The overall structure, shown in Fig. 22.5.1, consists of 12 interleaved 135MS/s 9-bit radix-2 SAR converters followed by a digital mismatch calibration unit. Each SAR resolves 9 bits in 12 clock cycles. The  $1V_{pp-diff}$  input signal is delivered to the sub-ADCs via a 1.7V buffer in order to limit kickback noise. Each SAR embeds its own T/H circuit, and bottom-plate sampling is used to reduce charge injection. The top plate sampling switch is a transmission gate which uses low- $V_t$  high performance analog (HPA) transistors to reduce  $R_{on}$  input signal dependency and thus, keep a good linearity (Fig. 22.5.2). In order to reduce the area while preserving good ratios between the capacitors, a compact, custom layout, lateral structure is used in the 9 bits radix-2 capacitive DAC as illustrated in Fig. 22.5.2 [4, 5]. The common bottom plate consists of a metal comb connected to the input of a latch comparator. The capacitor top plates are made of several metal fingers inserted into the bottom plate comb structure. The capacitor values are proportional to the number and the length of the fingers. The top plates can either be connected to the reference voltages  $V_n=250mV$ ,  $V_p=750mV$ , and  $V_m=500mV$  or the input signal  $V_{in}$ . The sequence of conversion steps shown in Fig. 22.5.1 is managed by the SAR logic that generates the control signals for the comparator and for the switches.

The 9-bit samples from the 12 interleaved ADCs are delivered in parallel to the digital mismatch calibration unit that runs in background in order to track mismatch variations. The calibration requires the input signal to be wide sense stationary and bandlimited to the Nyquist frequency. There is no adaptive feedback loop, meaning the signal is corrected after a single iteration, eliminating the potential stability issues encountered with adaptive techniques.

Offset mismatch is cancelled by equalizing the averages of each sub-ADC output to the average of sub-ADC<sub>0</sub> output. The relative offset of one sub-ADC is estimated as the difference between the modified moving averages of its output samples and the ones of sub-ADC<sub>0</sub>. The estimated offsets are then subtracted from their respective sub-ADC outputs samples. A random sequence is added to the estimated offset before the subtraction to spread across the entire spectrum the residual offset mismatch spurs caused by rounding errors. The 12-bit offset-corrected samples are then transmitted to the gain mismatch calibration unit where gain mismatch is corrected. The relative gain each sub-ADC is calculated as the ratio between the modified moving average of its samples' absolute values and the modified moving average of sub-ADC<sub>0</sub>

samples' absolute values. Gain mismatch is corrected by dividing each sub-ADC's output by its corresponding gain estimate.

Skew mismatch calibration, which principle is illustrated in (Fig. 22.5.3), is performed in the last stage. Each sub-ADC output can be seen as a sum of an ideal signal and an error term proportional to the timing offset and the signal derivative. The ideal signal is orthogonal to its derivative, meaning that averaging the product between the sub-ADC output samples and their corresponding derivative samples eliminates the ideal signal component while leaving a skew-dependent term. This term, proportional to the derivative power and the sub-ADC timing offset, is used in the skew calibration unit to recover timing skew estimates. The estimated error signal, calculated as the product between the derivative and the timing skew estimate, is then subtracted from the sub-ADC output to recover the ideal samples [6]. The signal derivative is obtained by passing the TIADC gain-corrected samples through a differentiating FIR filter [6], which coefficients were chosen such that its frequency response is accurate up to 750MHz. After skew mismatch calibration, the 12x12-bit digitally corrected signals are multiplexed and delivered at the output of the chip.

The test chip was fabricated using STMicroelectronics 40nm CMOS technology and is comprised of two of the previously described TIADCs (Fig. 22.5.7). The digital part has a 1.1V supply voltage similar to the analog core and the SAR logic. It was synthesized from a parametric C-code using Calypto Catapult C High-Level-Synthesis tool, making this flow quickly adaptable to any technology and any TIADC architecture.

Fig. 22.5.4 shows the measured performances versus input signal frequency. The SNDR progressively decreases from 51dB at DC to 48dB at a 750MHz input frequency, while the SFDR is higher than 62dBFS. The mismatch tones are kept below 70dBFS up to 750MHz. This is higher than previously published designs, which achieve, at best, 60dBFS [3] up to 90% of the Nyquist frequency. Above 750MHz, the performance deteriorates due to the limited accuracy of the derivative filter in that frequency range. For full scale sine inputs, the SFDR is ultimately limited by the harmonic distortion caused by the input buffer non-linearity. The THD is maintained below -58dB up to the Nyquist frequency. This is as good as previously published designs [1-3] that use additional linearity calibration circuitry. Fig. 22.5.5 shows the performances of the TIADC on a modulated signal, which is more likely found in practical applications. In this case, the buffer non-linearity is not a limitation, whereas mismatches create unwanted frequency components. At  $F_s=1.62GS/s$  the power consumption of the 0.83mm<sup>2</sup> TIADC including the digital background calibration, the references, and the input buffer is 93mW. The digital unit occupies 40% of the total area and consumes 53% of the total power when running continuously (Fig. 22.5.4). This overhead is offset by the achieved high SFDR and the ability to easily resynthesize the digital unit for any TIADC architecture or technology. In addition, the digital calibration energy overhead will decrease with CMOS technology scaling due to improved digital efficiency.

### Acknowledgement:

The authors would like to thank Andreia Cathelin and Borivoje Nikolić for their advice and support.

### References:

- [1] E. Janssen, *et al.*, "An 11b 3.6GS/s time-interleaved SAR ADC in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 464-465, Feb. 2013.
- [2] K. Doris, *et al.*, "A 480mW 2.6GS/s 10b 65nm CMOS time-interleaved ADC with 48.5dB SNDR up to Nyquist," *ISSCC Dig. Tech. Papers*, pp. 180-181, Feb. 2011.
- [3] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW Time-Interleaved ADC Achieving 50.9 dB SNDR and 3 dB Effective Resolution Bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 971-982, April 2013.
- [4] J. Bach, "Capacitive Array," *US Patent 7873191 B2*, May 2005.
- [5] S. Le Tual, *et al.*, "Integrated capacitive device and integrated analog digital converter comprising such a device," *US Patent Application 2013/0003255 A1*, June 2011.
- [6] V. Divi and G. Wornell, "Blind Calibration of Timing Skew in Time-Interleaved Analog-to-Digital Converters," *IEEE J. Selected Topics in Signal Processing*, vol.3, no.3, pp.509-522, June 2009.

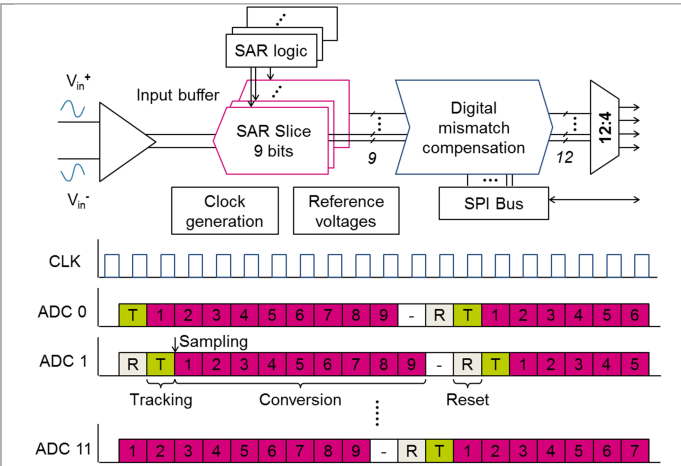


Figure 22.5.1: Overall structure of the Time-Interleaved ADC and sequence of conversion operations

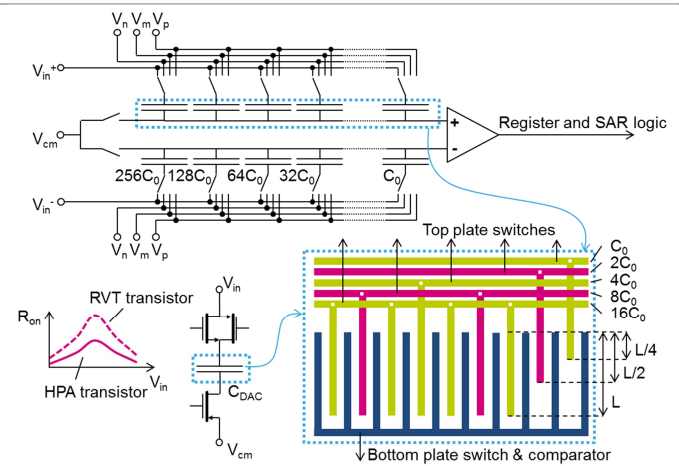


Figure 22.5.2: Bottom plate sampling and capacitive DAC schematic with lateral capacitor array layout (not entirely represented)

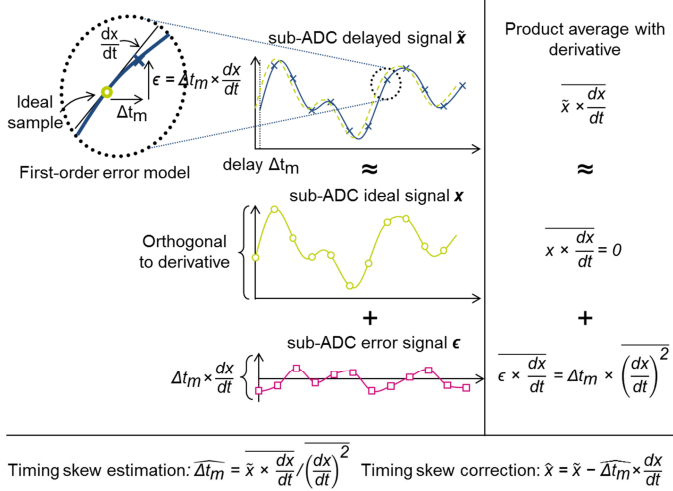


Figure 22.5.3: Skew mismatch estimation and correction principles

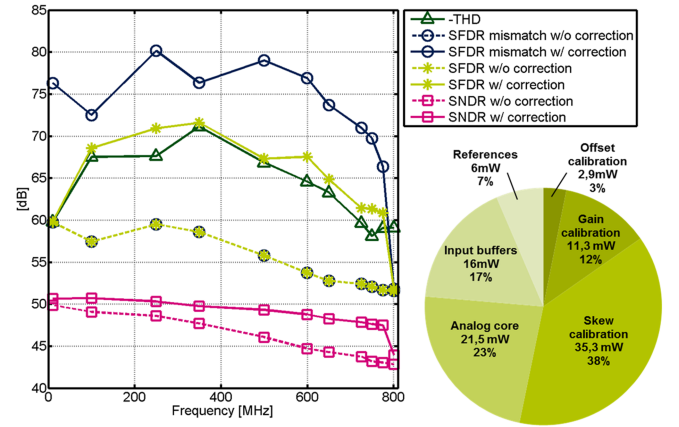


Figure 22.5.4: Performances of the TIADC over the Nyquist frequency range for a -1dBFS sine input and power consumption repartition

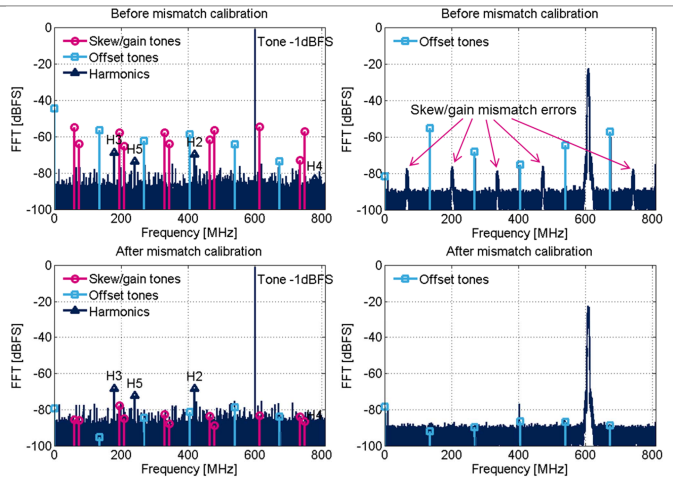


Figure 22.5.5: TIADC output spectrum before and after mismatch compensation with a sinusoid at 600MHz and a 10MHz bandwidth QAM16 modulated signal at  $F_{\text{carrier}} = 607\text{MHz}$

	ISSCC 2013 [1]	ISSCC 2011 [2]	JSSC 2012 [3]	This work
Technology	65nm	65nm	65nm	40nm
Sampling rate [GS/s]	3.6	2.6	2.8	1.6
Mismatch tones [dBFS]	50	55	60	70
SFDR [dBFS]	50	55	55	62
THD [dB]	-55	-58	-55	-58
SNDR [dB]	47	49	48	48
Power [mW]	795	480	44.6 <sup>(1)</sup>	93
FOM [fj/conv]	1207	801	76 <sup>(1)</sup>	283
Area [mm <sup>2</sup> ]	7.4	5.1	0.63 <sup>(1)</sup>	0.83

<sup>(1)</sup> without references and input buffer

Figure 22.5.6: Performance comparison with state of the art for input frequencies up to 90% of the Nyquist frequency

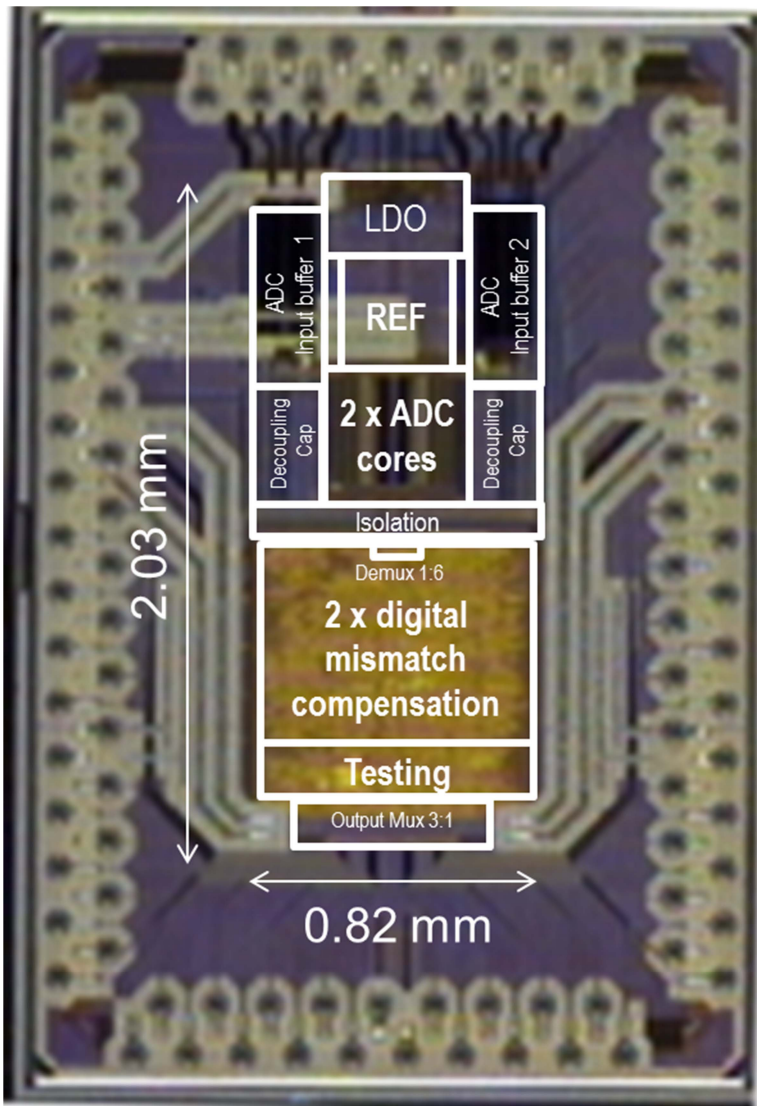


Figure 22.5.7: Photo of the die comprised of 2 x 0.83 mm<sup>2</sup> Time-Interleaved ADCs